



# Flip Chip Manufacturing at Aspen Technologies

## Overview

Design requirements for electronic systems are growing more complex and moving in very different directions compared to the past. However, there are two fairly similar requirements for next generation products. Interconnect density at all levels of the design must increase as dimensions grow smaller. In other words, more input/output signals must use less and less space. At the same time, performance must increase due to components operating at higher speeds.

During the design cycle, electronic products that have more signals and require better signal integrity, find limitations are caused by wirebond connections at the package level. Flip chip technology relieves many of the design constraints compared to wirebond, and has two key advantages.

1. Greater interconnect density
  - a. More input/output (I/O) signals per unit area
2. Better electrical performance at higher speeds
  - a. Lower resistance, capacitance, and inductance

These two advantages have been the primary drivers of flip chip technology. Based on certain assumptions for specific applications, other advantages can come into play. Flip chip can be lower cost and higher reliability, for both low I/O count consumer applications, and leading edge high I/O count devices.

Aspen Technologies has a great deal of experience with a wide range of flip chip technologies, to meet diverse design requirements. We develop and produce flip chip packaged devices for many different commercial and industrial markets. Our world class ability to utilize the right flip chip materials and processes for your product is available today.

## Trends

Constant improvements to semiconductor IC (Integrated Circuit) devices have a fundamental effect on flip chip technology. IC's of smaller size, new materials, and greater performance must be enabled by advances in flip chip packaging. Therefore, roadmaps of flip chip technology are almost always aligned with IC roadmaps.

- Smaller IC dimensions must have higher interconnect density, and drive flipchip package technology to provide smaller features, bump size, and bump pitch.

- The use of new IC materials, such as low k dielectrics and copper metallization, force steady reliability improvements in flipchip materials and processes such as underfill and thinner die.
- High speed signal performance requirements, including power and ground planes, drive improvement to flip chip design layout and lower dielectric materials.
- In all cases, flipchip material and process costs must either decrease over time, or provide better functional and reliability performance at the same cost. This is a key advantage of working with Aspen Technologies, we understand how our customer markets value performance versus cost.

Legislative requirements to eliminate the element lead are affecting flip chip technology. The move to 'Lead Free', or RoHS (Reduction of Hazardous Substances), is a significant cost and reliability challenge. Looking further ahead, 'green' packaging will be the next challenge, for packaging technology that is environmentally friendly and minimizes resource usage. Aspen Technologies has developed lead free packages for our customers over the past 5 years.

Historically, flip chip technology has competed with wirebond technology for development money and capital equipment. This has kept flip chip at a lower level of usage, which keeps cost higher, and slows reliability improvements. The migration from wirebond to flip chip processes is moving faster, as a significant number of products are finding flip chip technology is the only solution for better functionality, smaller form factor, and even lower cost.

## Process and Materials

Figure 1 illustrates some of the major flip chip assembly process steps, and Figure 2 shows a cross sectional representation of solder based flip chip packaging.

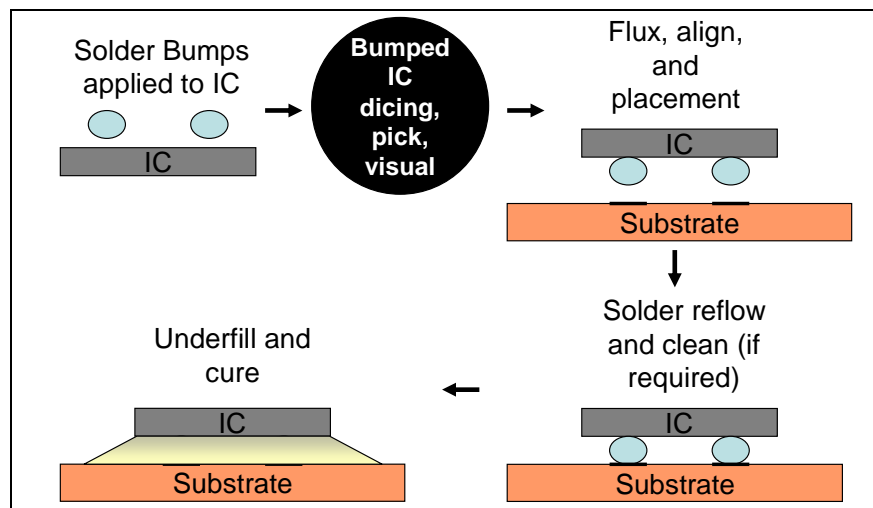


Figure 1: Typical solder flip chip packaging process steps

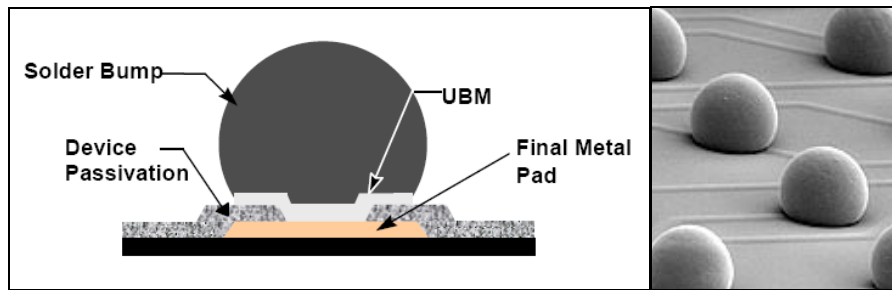


Figure 2: Solder bump cross section and SEM

Many different sets of materials and processes can be called flip chip technology. The variety can be confusing, and selection of specific materials must be addressed at the start of any flip chip package design cycle. Substrate selection, bump type, and underfill material between substrate and IC are three of the most important choices to make.

Table 1 is a list of the different material sets and processes used in the majority of flip chip applications today. A list of possible materials and processes follows.

- Bump Type

	<u>Material</u>	<u>Method</u>	<u>Process</u>	<u>Interconnect</u>
	<b>Solder</b>	Deposition	Evaporation	Reflow + Underfill
		Plating	Electro Electroless	
		Ball	Solder ball transfer Solder jet	
		Screen Printing	Solder paste deposition	
FLIP CHIP BUMP	<b>Au</b>			Conductive paste + underfill
		Plating	Electro	Reflow + underfill
				ACF
		Ball	Electroless	Thermocompression + underfill
			Stud bump	Thermosonic + underfill
			Pressure contact + non-conductive paste	
	<b>Polymer</b>	Screen printing	Cure	

Table 1: Flip chip bump technology overview

- Substrate Materials

Starting with selection of a substrate, different materials have unique behaviors over temperature. The substrate material effects on solder, underfill, and the IC must be thoroughly understood to produce a reliable device.

- Ceramic (many compositions)

- Silicon
- Organic
  - PCB
  - BT
  - Flex
- UBM (many compositions)
  - Sputter
  - Evaporated
  - Electroless Ni
- Solder deposition processes
  - Plated
  - Evaporation
  - Screen print
  - Jetting
- Solder deposition materials
  - Lead bearing
    - Eutectic lead / tin (37 Pb / 63 Sn)
    - High lead (>90 Pb)
  - Lead free (many compositions)
    - Tin/Silver and Tin/Silver/Copper
- Gold bump
- Gold stud bump
- Anisotropic adhesive
- Bump Design
  - Array, full or partial
  - Bump diameter
  - Bump height
  - Bump pitch
- Flip Chip Attach to create solder joints
  - Placement and reflow equipment
  - For solder, melting point +10-20 deg. C
    - Flux (many types)
      - Clean and no-clean
    - Solder paste
    - Inert or reducing atmosphere
  - Gold bump and gold stud bump
    - Thermosonic
    - Conductive epoxy
    - Anisotropic conductive epoxy
- Underfill Materials and Processes

- Cure and adhesion characteristics
- Flow characteristics
- Reworkability

Processes and materials must be carefully controlled to produce reliable flip chip packaged devices, guided by statistical process control. A standard 'control chart' is used, to measure the average value, and range of values, in a given process. After selection of upper and lower control limits, control charts give immediate feedback on a process, and if it is out of control. The goal of any SPC effort is not to detect out of control processes, but to prevent their occurrence in the first place. This is accomplished with capable processes, proven to produce acceptable results as a result of fully understood variation from common causes.

## Reliability

MTTF (Mean Time To Failure) is the primary reliability metric used to measure flipchip packaging technology. A finished part out in the field, that would not meet product specifications for performance over a specified lifetime, is a failure. If the failures are due to flip chip materials or processes, the failure mechanism must be determined, and a solution implemented before the flipchip packages are put in systems.

The different materials in a flip chip package, with internal stress changes over temperature, and TCE (Temperature Coefficient of Expansion) mismatch, are fundamental drivers of most failure mechanisms. Flip chip package reliability has been studied extensively over the past few years, and most failure mechanisms are well understood.

Figure 4 highlights some of the failure modes in a typical packaged flipchip IC, and Figure 5 shows a crack propagating through the solder ball after accelerated stress testing, such as temperature cycling. Typically, solder fatigue failure due to TCE occurs as an open (infinite resistance) due to cracks through the solder.

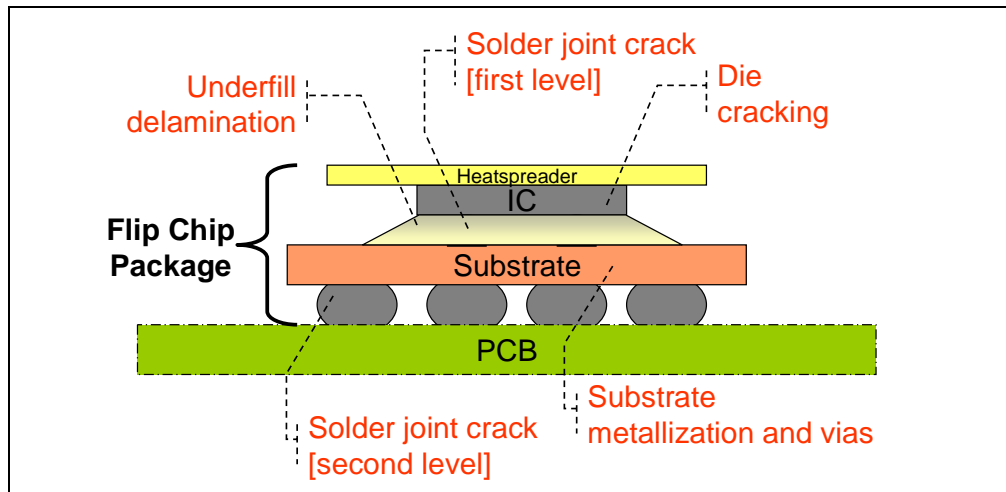


Figure 4: Typical flip chip failure modes

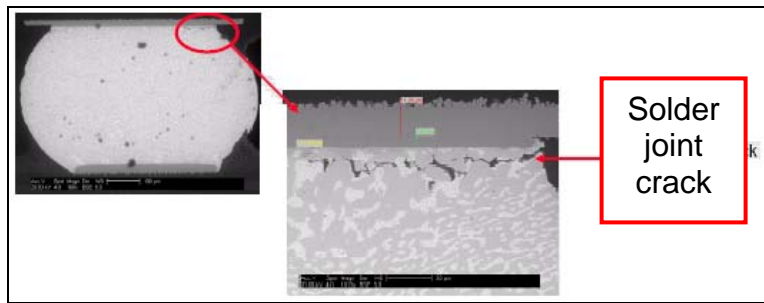


Figure 5: Solder fatigue failure mechanism

An important aspect of reliability performance is to overcome the thermal expansion mismatch between IC (silicon die) and substrate, when connected by the flip chip solder joint. Underfill materials bond the two surfaces together, to absorb stresses due to TCE, improving reliability and offering protection from moisture, ionic contaminants, radiation, and hostile operating environments such as shock and vibration. Selection of the optimum underfill material and process is one of the most important steps in the flip chip package design cycle.

#### Reliability characterization and testing

Many characterization tests are extensions of fundamental material property evaluations. For flip chip packages, a test usually evaluates the effect of assembly processes on the material(s) of interest. Characterization tests and flip chip materials are selected based on the end use of the product, such that not all characterization tests are done for a specific application, or set of materials, of a flip chip package. Characterization of solderability, voids, ball shear strength, and other tests can quickly provide results that apply to most applications and material sets. Aspen Technologies works with several service providers as required to quickly evaluate your design. Technicians are experts in performing the characterization tests, with state of the art equipment that is well maintained and fully utilized for the most accurate results at the lowest cost.

Flip chip package assembly processes need a high degree of control. As such, every process and material, must undergo proper qualification test procedures prior to its implementation. Reliability characterization and qualification testing are used to validate a specific set of flipchip package design and process parameters, and materials, in the finished product. Any change to form, fit, or function must undergo the same qualification tests to ensure acceptable reliability.

Qualification testing must accelerate the failure mechanisms of interest, without introducing invalid failure mechanisms. If a valid failure mechanism is found, changes to flipchip package design, materials, and assembly processes are made to obtain acceptable results from additional qualification testing.

Accelerated stress testing is a large part of reliability characterization and qualification tests. Stress testing is done to obtain reliability results in a short amount of time, rather than wait for field failures to occur. Table 1 lists many of the characterization tests, and accelerated stress tests that may be selected for a qualification effort.

	<i>Test</i>	<i>Conditions</i>	<i>Standards</i>
-	JEDEC pre-conditioning	Level 1 – 5	JSTD-020, JESD22
-	X-Ray / Sonoscan	Material cross section	
-	Warpage	Moire, optical, physical meas.	
-	Ball Shear		JESD22
T/C	Temperature Cycle	-65, -55, -40, 0 to 100, 125, 150 C; 500-1000 cycles; 20 – 30 min cycle time	MIL-STD 883, JESD22
HTS	High Temp Storage	100 to 170 C; 500 – 1000 hours	MIL-STD 883, JESD22
HAST	Highly Accel. Stress Test	130 C / 85% RH / 96 hrs	JESD22
THB	Temp / Humidity / Bias	125 C / 30 – 60%RH / V	JESD22
-	Alpha emission	(device dependent)	
P/C	Power Cycling	(device dependent)	JESD22
-	Mechanical testing	Drop, shock, & vibration	MIL-STD 883, JESD22
T/S	Thermal Shock	0 to 100, 125 C, 15 - 20 cycles	MIL-STD 883, JESD22
PCT	Pressure Cooker Test /Autoclave	121 C, 100% RH, 2 atm., 168 hours	JESD22
HTOL	High Temp Operating Life	125 to 150 C, V, 500 – 1000 hours	MIL-STD 883, JESD22
LTOL	Low Temp Operating Life	-10 to 0 C, V, 500 – 1000 hours	JESD22
ESD	Electrostatic Discharge	HBM, CDM, MM	JESD22

*Table 1: Reliability characterization and test summary*

#### Daisy chain die testing

To more effectively evaluate different flip chip design parameters and materials, accelerated stress testing may be done with a daisy chain die test vehicle. The test vehicle is used to ensure that assembled packages are quickly stressed, easily tested (open/shorts), and flip chip package failure modes will be well understood.

Daisy chain test vehicles for flip chip packaging have several characteristics that make them effective for reliability testing, accelerating the majority of failure mechanisms associated with a fully assembled flip chip package:

1. Ease of daisy chain die testing, with simple open/short DC test parameters.
  - a. Open daisy chain die connections, as a way to show catastrophic effects of stress on the assembled package.
  - b. Leakage testing can be done between exposed traces of opposite polarity, to determine corrosion and contamination mechanisms.
2. Ease of failure analysis by focusing on assembled package, without confounding effect of semiconductor IC device such as hot spots.
  - a. General flip chip thermo-mechanical stress effects
    - i. Solder ball crack
    - ii. Underfill adhesion
    - iii. Die crack in multiple directions

- b. Substrate degradation (traces and vias)
- 3. Fully characterized test vehicle to perform second-level (or system-level) stress testing, if required.

## Recommended Daisy Chain Die Test Vehicle



Figure 6: Daisy chain metallization between bumps

Die Size:	0.400 x 0.400 in. (10.16 x 10.16 mm) 1138 bumps, with 569 daisy chain pairs [each daisy chain pad/bump is electrically connected to one other daisy chain pad/bump and isolated from all others] Full array
Die thickness:	0.250 in. (0.635 mm) [thinner die are available, to customer specification]
Die metallization:	Al/Cu/Si (98/1/1) 0.9 microns thickness 0.0035 in. (0.089 mm) diameter
UBM:	Electroless Ni, ~ 5.0 microns thickness Immersion Au plating
Passivation:	Nitride 0.8 microns thickness
Bump 1:	Eutectic (63 Sn / 37 Pb) 200 micron pitch ~90 micron height
Bump 2:	Pb-free (95.5 Sn / 3.5 Ag / 1.0 Cu) [other Pb-free alloys are available] 200 micron pitch ~90 micron height

Let Aspen Technologies review your requirements and develop a strategy to quickly and effectively answer your flip chip questions. We use our experience and expertise every day to help customers just like you, delivering results that fit your budget and schedule.

Please contact Aspen Technologies for more information.

[sales@aspentechnologies.com](mailto:sales@aspentechnologies.com)

719-592-9100

[www.aspentechnologies.com](http://www.aspentechnologies.com)